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Characterizing Geometry-Dependent Crossover Frequency for Stripline Dielectric and Metal Losses

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Abstract

Digital signaling requires interconnects operating at microwave frequencies to achieve current data transfer demands in computing platforms. Therefore, the performance assessment of these interconnects is mandatory in order to visualize their range of usability and limitations so that a systematic design and implementation of prototypes and final products can be achieved. In this regard, the limitations of the interconnects are associated with two types of losses: i) those associated with signal reflections (mismatch), which are quantified through the return loss, and ii) those associated with physical losses originating from dissipation of energy, which are quantified by the insertion loss. Whereas both types of losses are important from a circuit design perspective, the latter is more important for material developers in the PCB industry. For this reason, in order to evaluate the suitability of a given material for particular applications within certain frequency bands, several figures of merit have been defined. The most commonly used terms in the PCB industry are the permittivity or dielectric constant (Dk) and dissipation factor (DF) of dielectrics, and the conductivity and surface roughness for metals. Nevertheless, until now there are no unique figures of merit that account for both dielectric and metal losses in a simultaneous way. A parameter like this can be very useful when identifying what PCB interconnect material(s) would negatively affect overall performance in a more accentuated way .

In this paper, the crossover frequency (CF) for the metal and dielectric attenuation curves is proposed as a figure-of-merit to indicate the frontier dividing the frequency band where the dielectric losses overpass metallic losses and vice versa. Particularly, striplines are analyzed here in order to avoid introducing parameters such as the filling-factor requirement for studying multi-dielectric configurations (e.g., microstrip lines). The importance of the CF parameter relies on the its ability to determine material performance by comparing the corresponding losses with those introduced by either the metal or dielectric counterpart. Thus, when considering a fixed PCB substrate thickness, similar widths for striplines would be required to obtain target impedance in different materials. In this case, higher CF would indicate superior dielectric performance. Similarly, when scaling down the substrate thickness and keeping the material properties constant (and maintaining the corresponding losses), the stripline dimensions should be reduced accordingly, thereby increasing CF and indicating that the metal losses would be dominant in a wider band. This paper will explore the variation of CF with geometry, materials, and structure (e.g., metal roughness) for striplines. This would point out the usefulness of this parameter to provide the designer with information about the main loss factor attributed to a given PCB interconnect. With this information, the designer can make an informed decision on selecting a cost-effective solution for a certain application, and in addition the material developer would get feedback to meet the requirements for the materials forming the interconnects.

Authors Biography

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1 Introduction

The selection of appropriate PCB materials is the first step towards the development of a successful circuit design. In the past, this selection was based primarily on mechanical and thermal considerations because there were no significant problems encountered from the electrical routing of the signal and power paths at relatively low data rates. As data rates have increased to reach transfer levels in the range of gigabits per second, accounting for fundamental transmission line concepts in circuit design has become mandatory. In this regard, the corresponding delay and losses introduced by the non-ideal properties of the media where the signals propagate affect the integrity of the digital information sent from one point to other within a circuit. Thus, it is important for the circuit designer to minimize these effects by selecting appropriate materials for implementing interconnect channels operating at a given bandwidth.

On the other hand, it is important to bear in mind that the PCB industry is largely driven by cost-benefit considerations. Although advanced dielectric substrates and metal foils are available to implement high-performance PCBs, these top-of-the-line solutions are not always the most appropriate for all applications. For instance, one would not use ultralow-loss dielectrics to implement circuits operating at slow data-rates. The circuitry would perform to specification with the use of typical FR4 laminated with rougher metal foils.

In order to aid the selection of an appropriate combination of materials, the performance characterization should begin with the determination (or at least an estimation) of the separate contribution of the conductor and dielectric losses to the total attenuation occurring on a PCB interconnect. Recently, much research has been performed in this direction based on the fact that dielectric and conductor loss data present different functional forms when plotted versus frequency [1]. The corresponding models may include several terms accounting for the different effects that occur when the signal is interacting with the media where the channel is implemented [2]. Even more elaborate models may be implemented by processing experimental data, thus providing a good idea of the contribution of each type of material loss to the attenuation [3]. On the other hand, simpler models are handy when limited bandwidths are being considered or when higher order effects such as the conductor-dielectric surface roughness introduces little change in desired properties. In this particular case, the dielectric losses can be considered proportional to frequency and conductor losses proportional to the square root of the frequency [4]. However, this approximation is only applicable to a very limited number of cases in PCB technology that is constantly evolving and dealing with continuously increasing data rates.

In spite of the afore-mentioned efforts geared at providing a unified and generalized methodologies to separating the dielectric and conductor losses, much work remains to be accomplished on this subject. In fact, a recent DesignCon paper [5] clearly stated the difficulties entailed in separating these losses due to the fact that additional resistance related to the surface roughness introduces frequency dependent effects that may present similar trends to those observed on the dielectric. In fact, due to the random nature of the surface roughness, most models are either based on empirical equations [6] or based on statistical data [7]. For current technologies, a proper use of these models allows for an accurate representation of the conductor attenuation and may eventually be used to determine the dielectric losses when the total attenuation is known. Furthermore, once the conductor and dielectric losses are known, it is possible to determine the frequency at which the dielectric attenuation surpasses the conductor attenuation. The use and importance of this frequency point as a figure-of-merit is analyzed in this paper.

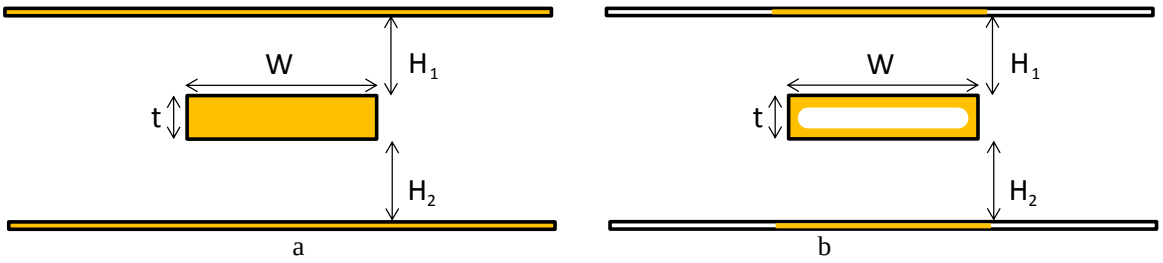


Figure 1. Conceptual sketch illustrating the current distribution (in yellow) within the cross section of a stripline with equidistant ground planes under DC conditions (a), and once the skin depth is smaller than the thickness of the trace (b).

To develop the concept proposed in the previous paragraph, this paper reports in-depth analysis based on physical experiments and full-wave simulations of striplines. We focus on stripline structures in order to avoid the variations in manufacturing and additional effects occurring in microstrip lines (e.g., frequency-dependent filling factor).

Losses in a transmission line

Signal power losses represent one of the main concerns for signal integrity engineers, especially as data rates increase and the cross sectional area of interconnects shrink. Therefore, when designing a PCB, mismatches in electrical transitions, parasitic effects, and unwanted coupling effects are avoided as much as possible. However, the intrinsic material losses cannot be avoided and should be taken into consideration from the early stages of the design process. In this regard, high-speed signaling interconnects are treated as transmission lines affected by losses that can be separated into three main categories: conductor losses, dielectric losses, and radiation. For striplines and at the frequencies of interest in this paper, losses due to radiation can be considered much smaller in comparison, so we can associate the experimentally obtained attenuation with just the conductor and dielectric losses.

Conductor Losses

These losses are associated with the finite conductivity of the traces used to form the interconnects. Thus, the corresponding resistance dissipates power due to the joule effect, a known issue at high frequencies. Moreover, as the industry of electronics is evolving towards higher density interconnects and packages, the cross section of interconnects are being considerably scaled down. This comes with a corresponding increase of the resistance associated with the metal traces, which can be obtained (assuming DC conditions) as:

$$R_{DC} = \frac{\rho\, L}{A} = \frac{\rho\, L}{wt} \qquad (1)$$

where ρ is the resistivity of the conductor material (usually copper), A = wt, and L, w and t are the trace's length, width, and thickness, respectively. Notice that in this equation (1), the resistance associated with the return path is neglected since the corresponding width is much larger than the width of the metal trace. Fig. 1a illustrates that the current can be assumed to be homogeneously distributed in the cross section of a stripline.

For current PCBs and packages, R_{DC} is very low due to the relatively large cross section of the interconnects. However, as frequency increases, the effective area from which the current is flowing is reduced due to the skin effect, which increases the resistance and consequently the signal attenuation. This reduction only occurs when the skin depth (δ) of the conductor used to

form the interconnect becomes comparable to its dimensions. In this case, a way to incorporate the skin effect into the model for the resistance requires a mathematical representation of the skin depth; this is:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2}$$

where ρ is the resistivity of the material conductor, f the frequency and μ is the permeability of free space.

It can be demonstrated that a good first-order approximation for determining the frequency-dependent cross-sectional area A in (1) is achieved by utilizing δ in the following fashion. For a typical PCB stripline $w>t$; A would be first modified by a change in thickness once $\delta \leq t$. In this case, the resistance of the signal trace can be represented by means of the following equation:

$$R_{AC\_trace} = \frac{\rho\, L}{2\delta w} \tag{2}$$

where t in (1) is substituted by 2δ due to the skin effect at higher frequencies where current is confined to the upper and lower edges of the metal trace, as illustrated in Fig. 1b. As expected, $R_{AC\ trace}$ is proportional to the square root of frequency due to its dependence on δ. Bear in mind, that in an actual interconnect the skin effect impacts the current distribution in all directions and within all the metals forming the interconnect. Furthermore, by assuming the use of smooth conductors and considering that the frequency is so high that the skin effect is simultaneously modifying the current distribution of the signal trace and the ground plane, it is reasonable to assume the following for the total AC resistance of the line:

$$R_{AC} \propto \sqrt{f}$$

or

$$R_{AC} = R_s \sqrt{f} \tag{3}$$

where R_s can be considered approximately constant at microwave frequencies. Thus, the increase of the resistance with frequency predicted by (3) yields that the conductor loss for lines with smooth surfaces are also proportional of the square root of the frequency [8]. Fig. 2 shows a curve illustrating the onset frequency of the skin effect (i.e. the minimum frequency at which the resistance becomes frequency dependent) for different standard foils used in PCB manufacturing. Since striplines are considered in this case, the onset frequency is determined when $\delta = t/2$. Notice that for all foils the onset frequency is below 1 GHz. For any high-frequency signals near the surface of the metal traces, the profile of the surface becomes an important factor to be considered when determining the conductor losses.

As it is widely known, the presence of roughness in the conductor material is necessary to improve adhesion to dielectrics in order to avoid delamination. Currently, there are different types of copper foils which present values of rms roughness (h_{rms}) from less than 5 microns to 10 microns; some of the most representative are shown in Fig. 3 [9]. Accurately modeling the surface conductor roughness is fundamental to accurately predicting the interconnect performance since the contribution of the surface roughness effect at high frequencies can reach 10%–50% [8,10].

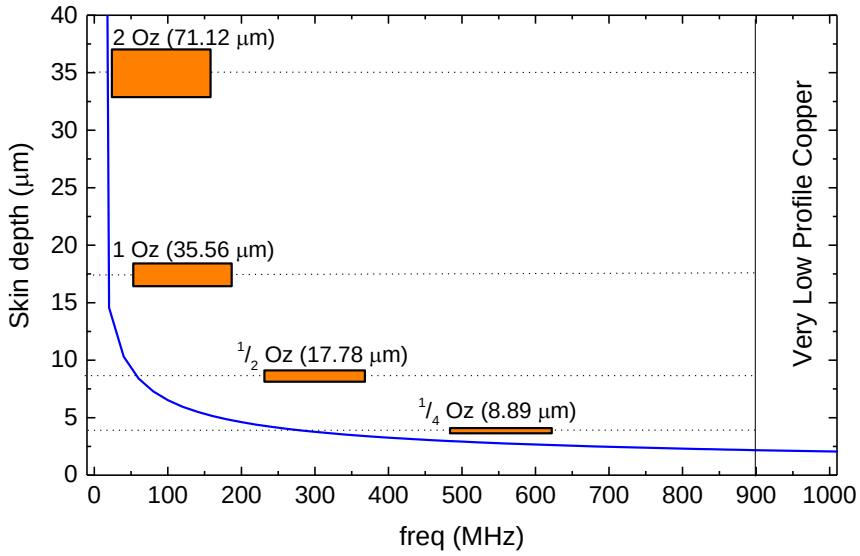


Figure 2. Skin depth versus frequency curve for copper illustrating the onset frequency for the skin effect for standard foils used in PCB technology (striplines are considered).

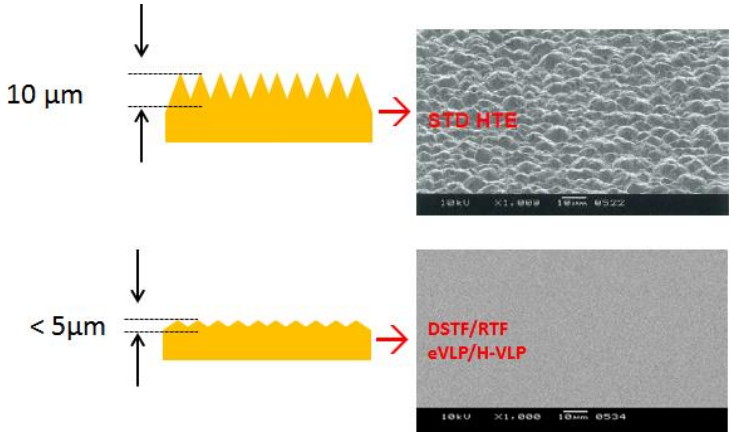


Figure 3. Illustration of different copper profiles currently used in PCB technology.

Much work has been reported over the last three decades about the losses introduced by the imperfect surface of metal traces. Three of the most popular models among engineers for considering this effect are:

1. Hammerstad & Jensen's (HJ) model [5, 6].
2. HJ Modified model [5].
3. Huray's snowball model [5, 7].

These three models assume that the AC resistance of the line is further increased by an additional factor K_H, which implies that (3) has to be modified to $R_{AC} = K_H R_s \sqrt{f}$. This in turn implies that the following expression can be written for the attenuation associated with the conductor losses:

$$\alpha_c = K_H K_c \sqrt{f} \tag{3}$$

where K_c is assumed to be approximately constant and K_H is a frequency dependent factor. Thus, the difference between the three models mentioned above relies in the way K_H is represented as a function of frequency. Notice that for a trace with smooth surfaces, K_H = 1. At frequencies at which the skin depth is much larger than h_{rms} also K_H = 1 since the impact of the surface roughness is not significant. Nevertheless, K_H rises with frequency, thereby increasing R_{AC} when the current flows in the cross-sectional area substantially modified by the surface roughness.

For the case of the HJ model, an empirical relationship between h_{rms} and K_H can be found; this is:

$$K_H = 1 + \frac{2}{\pi}\operatorname{atan}\left(1.4\left(\frac{h_{rms}}{\delta}\right)^2\right) \tag{4}$$

When Hammerstad and Jensen proposed (4), they noticed that for frequencies so high that $\delta \ll h_{rms}$, the interconnect's resistance increases up to twice the resistance of the same interconnect but with smooth surfaces. Thus, beyond a certain frequency, K_H reaches a saturation value of 2 (i.e. $1 \ll K_H \ll 2$). Years later, this was observed as an underestimation of the impact of surface roughness at high frequencies for conductors with extremely rough surface profiles [5, 7]. For this reason, a corrected equation was proposed to improve the HJ model, which is given by

$$K_H = 1 + \frac{2}{\pi}\operatorname{atan}\left(1.4\left(\frac{h_{rms}}{\delta}\right)^2\right)(RF - 1) \tag{5}$$

This second model is known as the HJ modified model, where the correction roughness factor (*RF*) may take values higher than 1; obviously considering *RF* = 2 yields the classical HJ equation (4) [5, 11]. The disadvantage of (5) is the lack of a generalized method by which to obtain *RF*. In order to overcome this inconvenience, the Huray method was proposed [7, 12], which uses a representation of the surface roughness through small spheres in flat hexagonal area cells. These cells are distributed throughout the surface of the metal trace, thus allowing for the following equation to be obtained:

$$K_{Huray} = \frac{A_{matte}}{A_{flat}} + \frac{3}{2}\sum_{i-1}^{j}\frac{N_i 4\pi a_i^2 / A_{flat}}{1 + \delta/a_i + \delta^2/a_i^2} \tag{6}$$

where A_{matte} is the surface area, A_{flat} is the surface area of the hexagonal cells, N_i is the number of spheres per cell, and a_i is the sphere radius. Since the accuracy of this model depends on the number and radius of the spheres, it is more computationally efficient when all the feature dimensions of the surface profile are known [5, 7]. It is important to mention that even though the accuracy of (6) is high when appropriately defining the corresponding parameters, (4) and (5) present the advantage of being more easily implemented and provide acceptable results at frequencies of gigahertz (< 20 GHz) for current technologies.

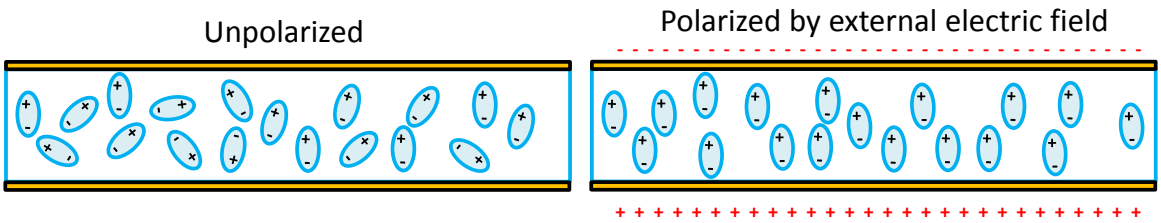


Figure 4. Illustration of the polarization phenomena in a dielectric.

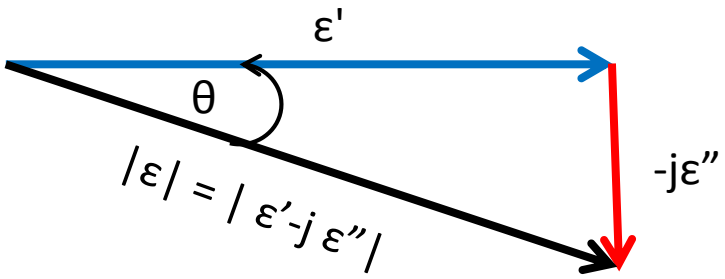


Figure 5. Graphical interpretation of the loss tangent or dissipation factor with two-dimensional vectors.

Dielectric Losses

Dielectric losses are associated with the dissipation of energy in the dielectric substrate and can be grouped into two main categories: losses due to polarization currents and losses due to conduction currents. Whereas the latter is negligible on PCB dielectrics, losses due to the polarization of the dielectric are significant at microwave frequencies. In order to explain the polarization phenomena, dielectric materials can be thought as a cluster of closely spaced electric dipoles. These dipoles react to signals by vibrating when tending to align with the associated time-varying electric field (see Fig. 4). During this process, energy is both stored and absorbed by the material thereby contributing to signal delay and attenuation. In fact, as frequency increases, the losses increase because more energy per unit time is absorbed.

The parameter that allows for the quantification of the delay and attenuation occurring in a dielectric media is the complex permittivity [1]:

$$\varepsilon = \varepsilon' - j\varepsilon'' \tag{6}$$

From a signal integrity engineer's point of view, the real part ε' quantifies the speed of propagation (i.e., the higher ε' the slower the propagating signal), meanwhile the imaginary part $-\varepsilon''$ relates to the losses occurring in the material. For characterization purposes, the dielectric losses can be described by the so called loss tangent ($\tan\theta$) or dissipation factor (DF), which is the ratio of the imaginary to the real part of the complex permittivity. Fig. 5 shows a graphical interpretation of this parameter that is expressed by:

$$DF = \tan\theta = \frac{\varepsilon''}{\varepsilon'} \tag{7}$$

In PCB dielectrics, *DF* is a parameter that dramatically depends on the resin content, resin type, frequency, and effects associated with the fiber glass weave.

Considering DF, an expression can be written for the attenuation due to the dielectric losses; this is [13]:

$$\alpha_d = \frac{DF \times \beta}{2} \tag{8}$$

where β is the phase delay given by the imaginary part of the propagation constant (γ). Thus, assuming a weak variation of *DF* and ϵ_r with frequency (which implies that β is a linear function of frequency), which is a reasonable assumption for the purposes of this research; the following alternative expression can be written for α_d:

$$\alpha_d = K_d f \tag{9}$$

In (8), K_d is a proportionality constant. This expression (9) together with (3) will quantify the crossover frequency as explained in the following sections.

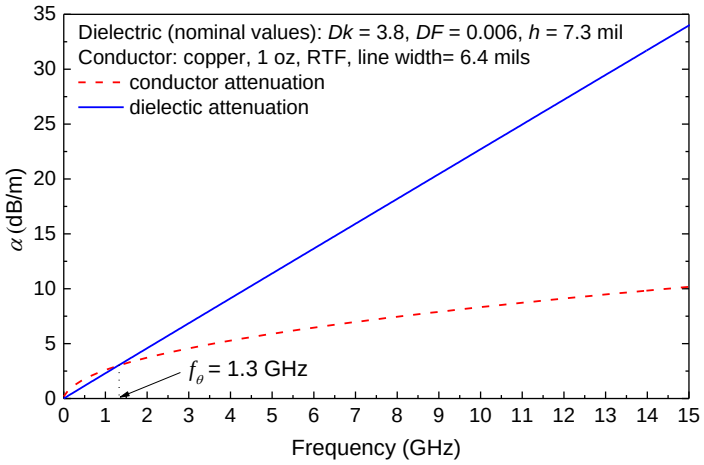
Crossover frequency: definition and determination

At microwave frequencies, it is possible to express the total attenuation occurring in a PCB transmission line by means of

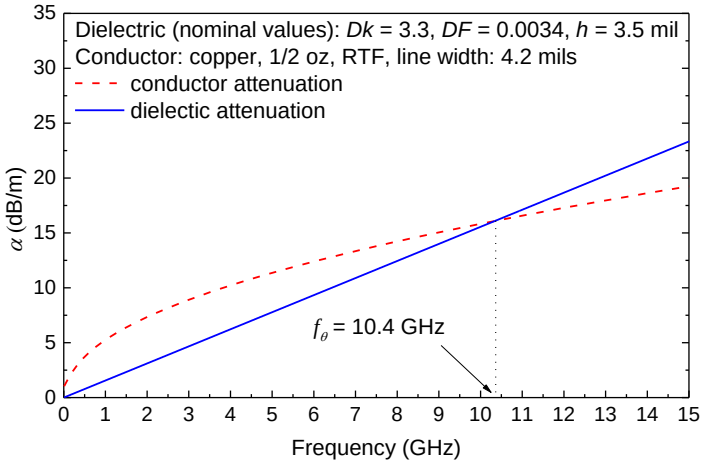
$$\alpha = K_H K_c \sqrt{f} + K_d f \tag{10}$$

where (3) and (9) are used to represent the conductor and dielectric losses respectively. When selecting the most appropriate combination of PCB substrate and copper foil for a particular application, it is important to determine which one of the two terms on the right hand side of (10) is more significant within the frequency range of interest. Thus, when the term related to the dielectric losses is significant and even higher than that related to the conductor losses, the designer may consider to ask the PCB supplier for a substrate material with reduced losses. It is tempting to assume that when the opposite occurs, thicker copper foils with diminished surface roughness would improve the interconnect performance. Well, this is not always the case; because thickening the copper foil would only reduce the DC resistance of the lines and losses would be lowered only at low frequencies. Similarly, reducing the surface roughness of the metal traces within certain limits may present only a small improvement on the interconnect characteristics if the dielectric losses are too high. Thus, knowing the frequency at which the contribution of the conductor and dielectric losses to the total attenuation is the same, makes it possible to improve the performance of the interconnect by changing the characteristics of either the dielectric or the metal below or above this frequency. Moreover, the sensitivity of the crossover frequency to changes in materials and geometry of the interconnect provides information about the corresponding benefits of these changes. This sensitivity analysis is discussed in greater detail later in this paper.

The crossover frequency (f_θ) is defined as the frequency at which $\alpha_c = \alpha_d$ [4]. Thus, due to the shape of the curves related to each one of these attenuation components, the dielectric losses surpass the conductor losses beyond f_θ. This is graphically shown in the plots on Fig. 6. Notice that for the particular example illustrated in this figure, reducing *DF* by ~35% increases f_θ by one order of magnitude. Nevertheless, it is necessary to mention that from a material fabrication process, it is difficult to modify *DF* while maintaining *Dk* constant. Therefore, the cross section of the line has to be modified accordingly to retian the target impedance. In Fig. 6, for instance, the substrate with lower dielectric loss is thinner and also exhibits a lower permittivity. In this case, the 50-Ω stripline is narrowed compared to the strip width on the other substrate. This



(a)



(b)

Figure 6. Crossover frequency for 50-Ω striplines lines fabricated on different PCB substrates.

implies that the conductor losses are also higher, and this contributes to further increasing the crossover frequency. Although in general terms a reduction of the dielectric losses would increase f_θ, it is necessary to analyze in a systematic and controlled way, the corresponding impact of changing the material properties and geometry.

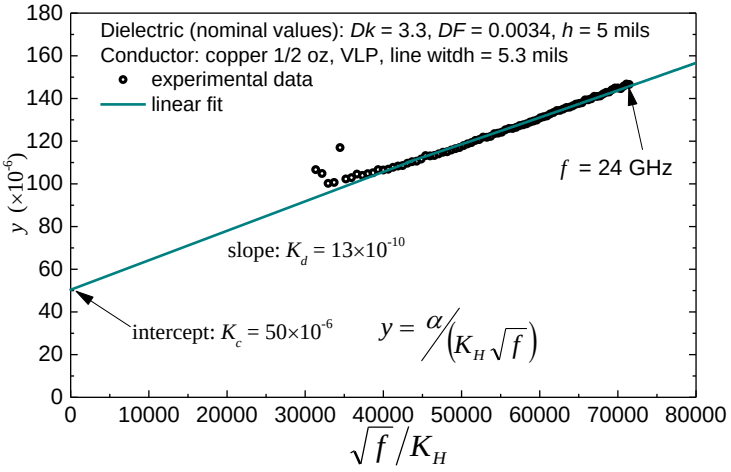
In this work, two approaches are applied to obtain the crossover frequency: i) directly from experimentally obtained attenuation data, and ii) using full-wave simulations.

Determination from experimental data

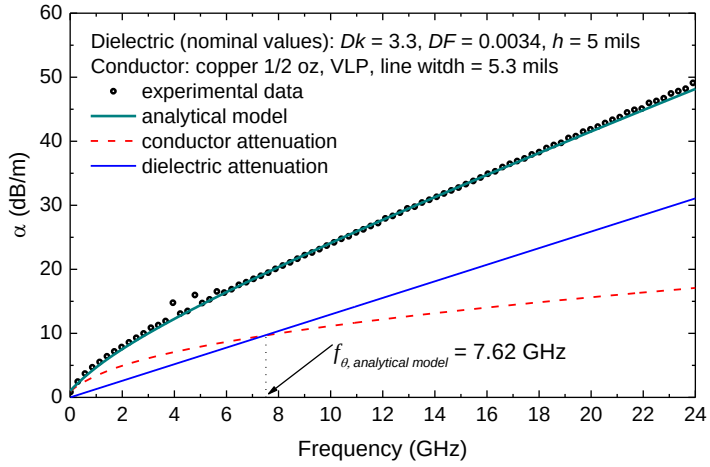
When determining f_θ from experimental data, the first step is obtaining the curves that represent the separate contribution of the conductor and dielectric losses from the total transmission line loss. In this case, experimental attenuation versus frequency curves is used to determine the attenuation components due to the conductor and dielectric losses. For this purpose, the following formulation is employed. Firstly, (10) is divided by the product of $K_H \times \sqrt{f}$, which yields:

$$\frac{\alpha}{K_H\sqrt{f}} = K_c + K_d\frac{\sqrt{f}}{K_H} \tag{11}$$

Notice that this step allows for the consideration of (11) as the equation of a straight line, where $y = \alpha/K_H\sqrt{f}$ and $x = \sqrt{f}/K_H$ represent the dependent and independent variables, respectively. It is important to point out the fact that K_H is obtained by applying (5), whereas K_c and K_d are considered as constant as explained when defining (8) and (9). Therefore, performing a linear regression of y versus x data, K_d and K_c can be obtained from the slope and intercept with these ordinates, respectively. Bear in mind that considering the appropriate model for the effect of surface roughness is fundamental to obtaining accurate and meaningful results. In fact, either ignoring the impact of surface roughness or misrepresenting it may lead to incorrect conclusions since the corresponding effect may be considered as part of the α_d curve. For this paper, the HJ



(a)



(b)

Figure 7. Determination of the conductor and dielectric attenuation curves from experimental data: a) regression for obtaining the model parameters, and b) model implementation.

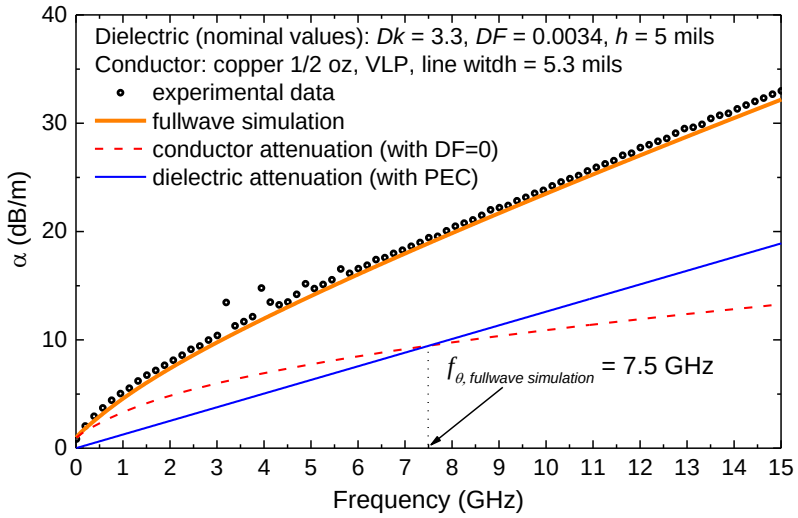


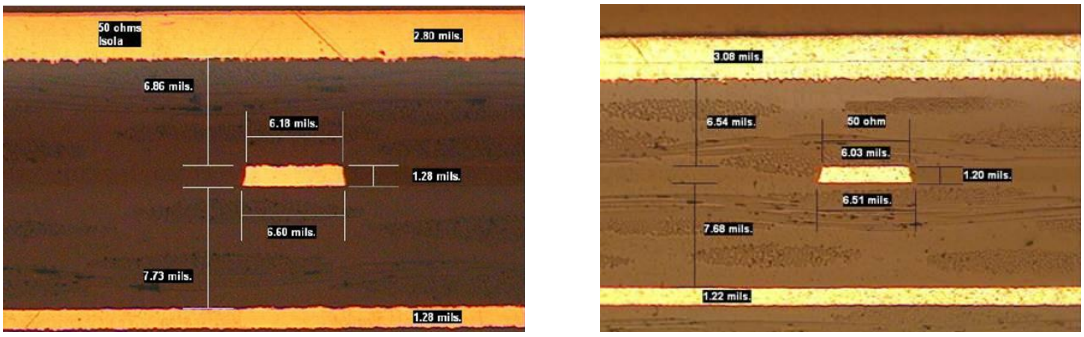
Figure 8. Correlation of full-wave simulations with experimental attenuation data for determining conductor and dielectric attenuation curves.

Modified model in (5) was used, which accurately represents the metal surface roughness and simplifies the analysis [5]. The linear regression involving equation (11) is shown in Fig. 7a, where the obtained values are: $K_c = 50\times10^{-6}$ and $K_d = 13\times10^{-10}$. Fig. 7b shows that by using these values, the total attenuation versus frequency data can be accurately reproduced within the considered frequency range. Moreover, the conductor [equation (3)] and dielectric [equation (9)] attenuation curves are also shown in this figure, which allows for the straightforward determination of the crossover frequency.

Determination from full-wave simulations

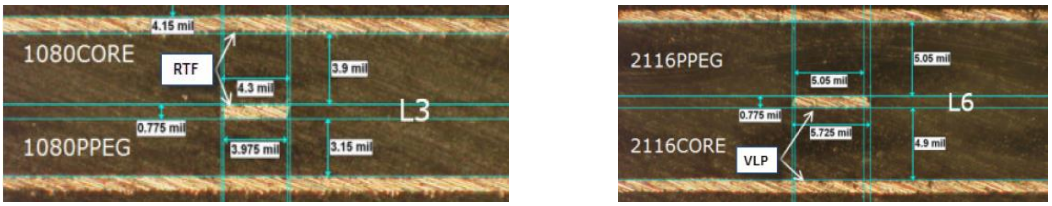
Even though obtaining f_θ from experimental data is desirable since measurements reflect the properties of the involved materials, a large number of prototypes would be required to carry out a systematical study like the one presented in this paper (e.g. multiple dielectric materials with different properties, copper foils, roughness profiles, etc.). Fortunately, the analysis can be carried out by carefully performing a series of full-wave simulations as explained shortly.

When the experimental attenuation per-unit-length of a stripline geometry is known, these data can be used as a target for calibrating a 3D model using a full-wave solver. For instance, on the prototype described in Fig. 8, the model for the attenuation is shown to be in agreement with the experimental curve after performing parameterized simulations considering the nominal specifications corresponding to the materials used to build the prototype. Once the model is calibrated, new simulations are carried out assuming that changing the dielectric properties does not affect the metal losses and vice versa. In this case, the conductor attenuation can be obtained by simulating the calibrated model after defining the dielectric as lossless (see red curve in Fig. 8). Likewise, the dielectric attenuation is obtained through simulations considering that the metals behave as perfect electric conductors (PECs). Notice that using the resulting curves, the value for f_θ is graphically obtained in Fig. 8, and approximately corresponds to the same parameter obtained from experimental data in Fig. 7. This procedure can be repeated by changing the properties of the involved materials to analyze the sensitivity of f_θ to these variations. In fact, the usefulness of this approach is explained below.



(a) (b)

Figure 9. Cross section of striplines on standard PCB material (Dk = 3.8, DF = 0.006) using different copper foils: a) RTF ($h_{rms} \approx 4$ µm), and b) VLP ($h_{rms} \approx 2$ µm).



(a) (b)

Figure 10. Cross section of striplines on high-performance PCB material (Dk = 3.3, DF = 0.003) using different copper foils: a) RTF ($h_{rms} \approx 4$ µm), and b) VLP ($h_{rms} \approx 2$ µm).

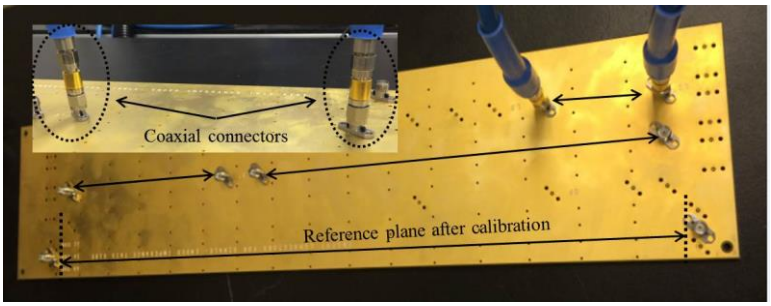


Figure 11. Photograph of one of the PCB prototypes detailing the location of the striplines.

Experiments

Varying length stripline configurations targeting 50 Ω impedance were implemented in four different prototype PCBs; two prototypes were fabricated using a mid-performance PCB laminate (nominal Dk = 3.8, DF = 0.006), and two more were fabricated on a high-performance PCB laminate used for microwave applications (nominal Dk = 3.3, DF = 0.0034). The difference between the two boards in each material is the surface roughness of the copper foils used; reverse treat foil (RTF) with rms roughness h_{rms} = 4 µm was used to laminate the mid-performance dielectric material, and very low profile (VLP) foil with h_{rms} = 2 µm was used to laminate the high-performance dielectric. The cross sections corresponding to the lines in each one of these prototypes are shown in Figures 9 and 10. Also, note the different cross-sectional area for the striplines in each case; the impact of this difference will be discussed in greater detail shortly.

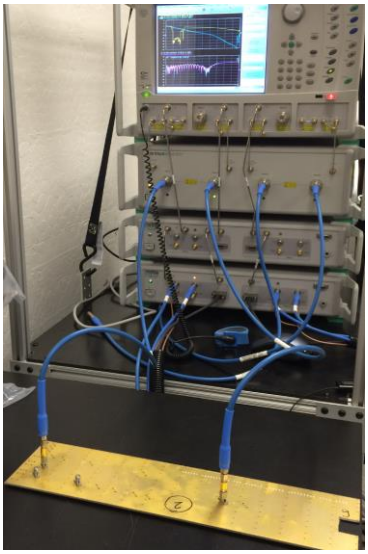


Figure 12. Setup configured to perform two-port S-parameter measurements.

Material type	Copper foil/profile	Stripline cross section	f_θ
Standard	1 oz/RTF	5,276 μm^2	1.3 GHz
	1 oz/VLP	4,854 μm^2	3.6 GHz
High performance	0.5 oz/RTF	2,068 μm^2	10.5 GHz
	0.5 oz/VLP	2,694 μm^2	7.6 GHz

Table I: Experimentally determined crossover frequency for the different fabricated prototypes. f_θ is affected in these prototypes not only by the changes in the dielectric properties and copper laminate but also on the stripline cross section and variations on dielectric properties (for instance, when fiber weave pattern changes).

In order to perform S-parameter measurements, coaxial K-type microwave connectors were attached to the boards to terminate the striplines and interface directly with the measurement equipment. Fig. 11 shows a photograph of one of the prototypes. Before performing the measurements, a vector network analyzer (VNA) setup was calibrated using a two-port electronic auto-calibrator, which establishes a reference impedance of 50 Ω and shifts the measurement plane up to the cable connectors to be matched with the prototypes. The setup is shown in Fig. 12. S-parameter measurements from striplines with varying lengths for all the prototypes were obtained. These measurements, include the effect of the connectors required to access the PCB traces. Therefore, a line-line algorithm was employed to obtain the per-unit-length propagation constant ($\gamma = \alpha + j\beta$) using the experimental S-parameters of two lines varying only in length [14]. This procedure effectively removes the parasitic effect of the connectors. Afterwards, $\alpha = \mathrm{Re}(\gamma)$ is obtained for each prototype so that f_θ can be experimentally determined as explained before. The corresponding results are shown in Table I. Notice that due to the difficulty of modifying only one variable (e.g., surface roughness, stripline cross section, dielectric properties, etc.), the direct use of measured data does not allow for performing a systematic analysis of the corresponding effect on f_θ. Instead, the experimental data was used to calibrate a 3D model, and then full-wave simulations were subsequently performed for this purpose.

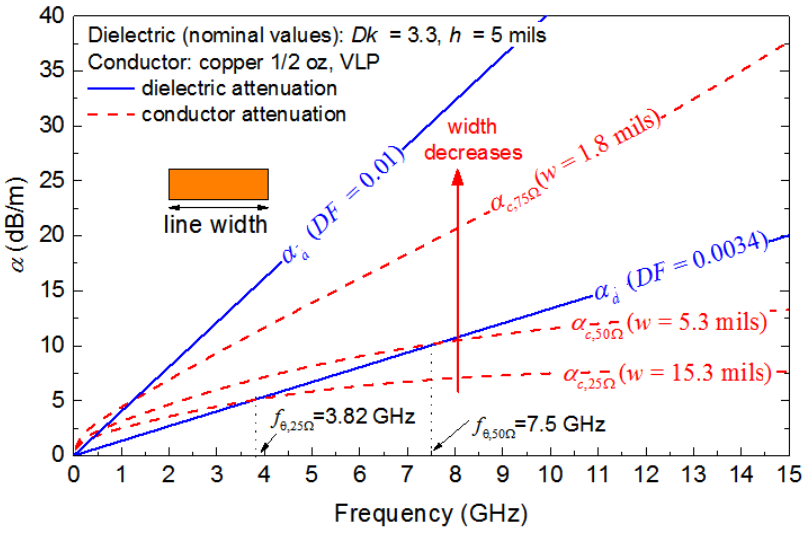


Figure 13. Determination of the crossover frequency for lines configured for different impedance assuming the same PCB conditions.

Impact of changing geometry and material properties on f_θ

The experimental data described in the previous section was used to calibrate a 3D model. In addition, we are assuming that changing the geometry and material properties one at a time allows for the identification of the corresponding impact on the dielectric and conductor losses, which in turn can be used to obtain the crossover frequency and study its variation with these parameters. The following subsections show the results of this analysis.

Stripline width

In this case, the copper foil properties are maintained constant throughout the simulations performed while considering different stripline widths for achieving characteristic impedances of 25 Ω, 50 Ω, and 75 Ω respectively. Fig. 13 shows the corresponding curves. As expected, higher characteristic impedance narrows the line and consequently increases the conductor losses. Therefore, when considering a high performance laminate with low dielectric losses, high values for the point of intersection for α_c and α_d are expected. Notice in Fig. 13, for the narrowest line there is no intersection between the separate attenuation curves. This point out the inconvenience of using 75-Ω impedance lines at these frequencies for these particular material conditions. An extreme case is also included in Fig. 13, where α_d for a second dielectric represents the loss of a regular FR-4 laminate (DF = 0.01). Observe that for the three considered impedance cases, f_θ is below 1.5 GHz, indicating that the dielectric losses are much higher than those associated with the conductor beyond this frequency. This strongly suggests the need of considering a better laminate within the required frequency range of operation.

Copper foil (trace thickness)

Now, the simulations are performed assuming constant characteristic impedance and different copper foils for two dielectric materials exhibiting different loss characteristics. Fig. 14 clearly illustrates the noticeable change in f_θ when considering a high performance laminate. As the copper foil is made thicker, there is more surface area for the current to flow through the cross

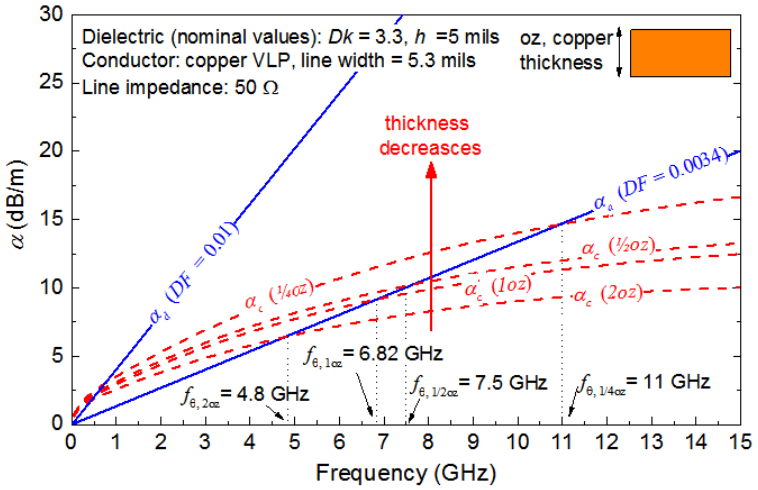


Figure 14. Determination of the crossover frequency for lines presenting different copper foil assuming the same PCB conditions.

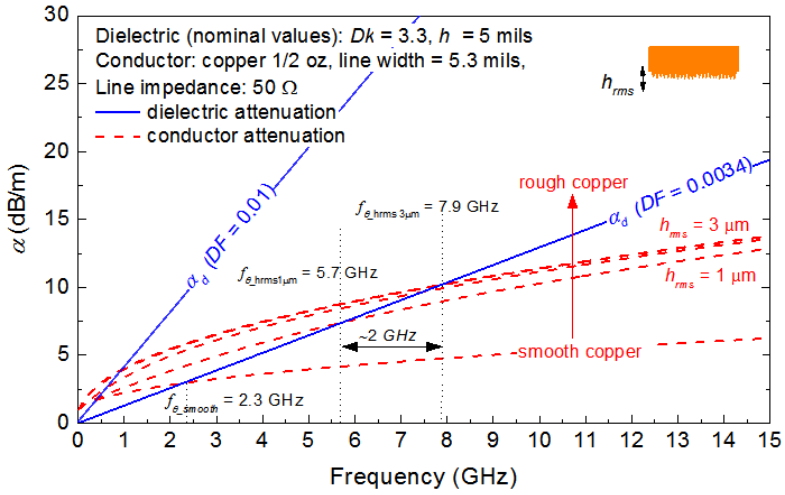


Figure 15. Determination of the crossover frequency for lines with different surface roughness and assuming the same PCB conditions.

section of the stripline even when the skin effect is accentuated. This approximately reduces 30% the conductor losses when changing the copper foil from ¼ oz to 2 oz. Nevertheless, this is only an effective solution when combining the extra copper with a high-performance laminate. As can be seen in Fig. 14, f_θ is significantly reduced (from 11 GHz to about 5 GHz) from the ¼ oz to the 2 oz foil for the low loss laminate. In contrast, a very small change in the crossover frequency is obtained for the lossier laminate material.

Copper profile (metal surface roughness)

Fig. 15 shows the simulation results when the surface roughnesses of the striplines are modified. Changes in this parameter also are more relevant from a practical point of view within the analyzed frequency range when considering a low loss dielectric material. An interesting result observed through comparing simulations is that for h_{rms} larger than 3 µm, no significant changes

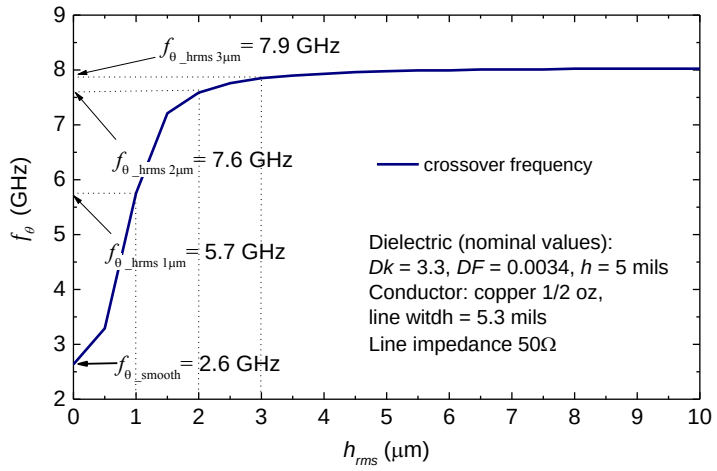


Figure 16. Crossover frequency versus h_{rms} showing the corresponding limits in current PCB technology.

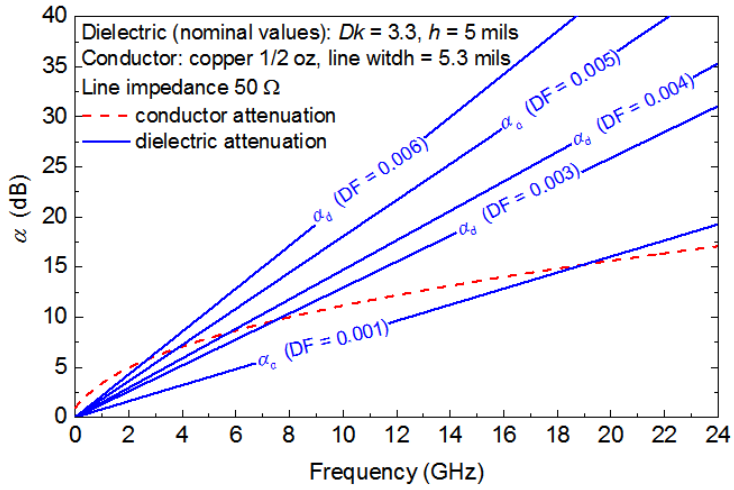


Figure 17. Determination of the crossover frequency for lines with different dielectric losses.

of the conductor losses are observed. In addition, notice that a significant reduction of f_θ is noticeable for values of h_{rms} < 2 μm, which points out the necessity of reducing this parameter below this value in order to improve the performance of interconnects for high-speed applications. The theoretical limit in this case is established by h_{rms} = 0 (i.e. a smooth conductor); for this particular example considering a low loss dielectric laminate, f_θ = 2 GHz, where $f_\theta \approx$ 7.6 GHz for h_{rms} = 2 μm. Thus, there still remains significant headroom for reducing the metal losses through smoothing the metal-to-dielectric interfaces. Fig. 16 verifies this fact through the inspection of the f_θ versus h_{rms} curve. Notice the significant change of the crossover frequency for VLP and RTF foils when using a low-loss dielectric laminate.

Dielectric loss

A final and complementary comparison is shown in Fig. 17, where different dielectric losses are considered. As the reader will infer from the previous comparisons, better dielectrics (i.e. with

lower loss) push f_θ out to higher frequencies and this parameter is very sensitive to improvements on the conductor properties. In contrast, lossy laminate materials will exhibit crossover frequency values at a much lower megahertz range, which points to poor performance at multi-gigahertz frequencies. Moreover, in the latter case, no substantial improvement in the performance of interconnects is expected when improving the characteristics of the metal foils.

Conclusions

PCB characterization experiments and simulations were carried out to show the usefulness of the crossover frequency for assessing the performance of striplines when considering changes in geometry and material properties. In lieu of conducting this systematic analysis entirely through prototype measurements which would require of a great number of samples with strictly controlled process parameters, it was shown that full-wave simulations are a viable characterization option provided that the 3D model is implemented through several model-experiment correlations.

Results highlight that low values of f_θ indicate poor dielectric performance and barely noticeable improvement of the interconnect characteristics when modifying the properties of the copper foil. In contrast, the attenuation due to the dielectric loss in high-performance laminates will not only surpass the conductor attenuation at frequencies of gigahertz, but also allows for a substantial improvement of the interconnection transmission characteristics when smoother copper foil profiles are used. This conjecture can be systematically identified through the determination of the crossover frequency. In fact, the results shown also point to the benefits of either reducing more the surface roughness of high-speed interconnects or fabricating using alternative printed interconnect processes in combination with advanced low loss laminates.

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