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Application Note

Sequential Lamination in Printed Circuit Boards

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Background

Sequential lamination is a variety of technologies, where already laminated subparts (or subcomposites) are laminated to additional layer of copper, or another subpart. A sequentially-laminated Printed Circuit Board (PCB) goes through at least two lamination cycles, and can go through many more. This build approach is the mainstay of High-density Interconnection (HDI) products and has been used in many forms. This technology as a whole has been very successful and today is essential for mobile communications and computer chip packaging, among many other uses. Many of these products are small, light and thin. This Application Note addresses the mechanical issues of this technology, when it is used on thicker boards.

There are a large number of different types or architectures for this technology. A few are briefly outlined here:

- **Standard HDI:** Thin center core (2-4 layers), with generally 1-3 sequentially applied circuit layers to each side. The outer layers are attached by microvias, the center core uses drilled through vias. This is the most common sequential lamination approach. This is a well understood technology and not covered in this note.
- **High Layer count HDI:** Thicker center subpart (6-26 layers, typically), with 1-2 sequentially applied circuit layers on each side. The layers are attached by microvia. The center cores have drilled plated through holes, called Buried Vias for connection. There are two categories for this paper:
  - Microvias are not stacked on the buried vias
  - Microvias are stacked on the buried vias
- **Blind via boards.** Two subparts are glued together, where the subparts are on the outside of the finished PCB. Subparts and finished PCBs have drilled-plated through holes. The surface layers may also have microvias.
- **Combinations** of the above technologies is common. All versions are not reviewed, as the issues follow the same pattern as the individual structure.

This technology is not without problems; particularly as it is combined with thicker PCBs and higher layer counts. There are a few general issues that have been associated with this technology: resin cracks, delamination, resin voids, and failed microvia connections.

Stress Factors and Failure Modes

One key difference is the way that stress builds inside these structures during thermal excursions. The major consideration in stress for all PCBs is the mismatch in thermal expansion between the three major components. Glass reinforcement has a Coefficient of Thermal Expansion (CTE) of about 6 ppm/°C, Copper has a CTE of 17 ppm/°C and the resin has a variable CTE depending on resin type but ranging from 100 ppm/°C below Glass Transition Temperature) (Tg) to 400 ppm/°C above the Tg (Refer to Figures 1 and 2). The copper-to-resin mismatch is key focus for this Application Note.

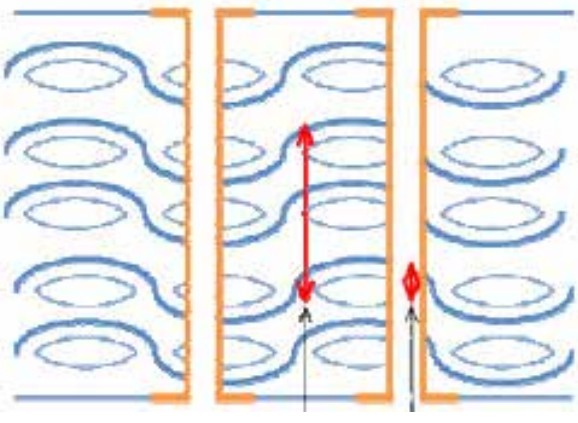

Figure 1

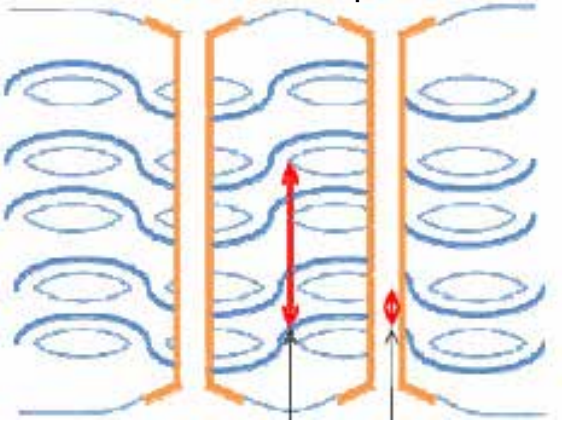

Figure 2

In the Z-axis, the resin glass matrix expands 4.5 to 5 times faster than copper below Tg, and 17 to 20 times faster than copper above the Tg. This causes the resin areas to swell around plated-through vias and is the cause of pad lifting on conventional PCBs. In conventional PCBs, the surface via pad is deformed into the air, so no permanent change occurs, except pad lifting or slight voiding under the surface pad.

In sequential laminated boards, the buried vias are inside more circuit board material, at least a glass/resin matrix and likely additional copper layers. This creates a new structure at this key stress point, which creates new ways for the stress to assert itself (Refer to figures 3 and 4). The way these structures handle stress is illustrated below:

HDI Structures

At Room Temperature

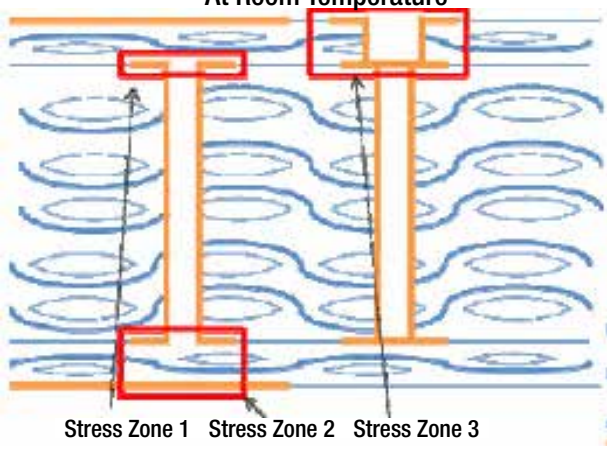

Figure 1

At Peak Reflow Temperature

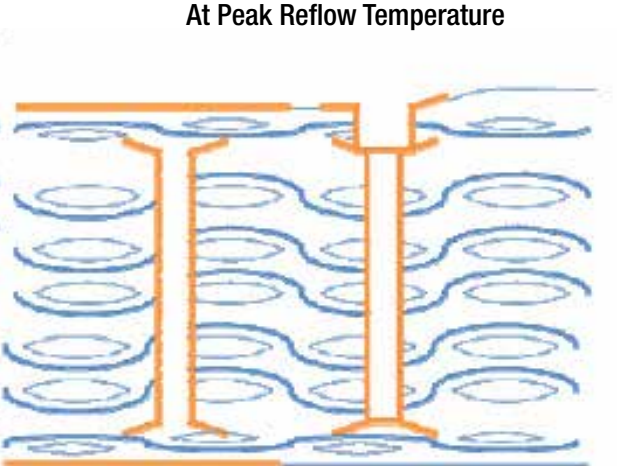

Figure 2

Stress Zone 1: Region above an embedded via (blind or buried) between the copper pad and the first layer of glass above the pad.

At the temperature rises, the dielectric surrounding the via expands faster than the copper via, causing two things:

1. Force is applied on the capping glass layer, which puts tensile stress on the copper resin interface on the via pad. In other words, it tries to pull the resin off of the pad.
2. The copper pad deforms, trying to lift at the edge. This can create additional stress and a leveraging or fulcrum to the stress from #1. This also can help create a shear vector X-Y axes) to the stress, that adds to the Z-axis vector from standard expansion.

The net effect is massive force exerted to the region around the embedded via surface pad. Since glass is strong in comparison to resin, it does not relieve any of the stress, effectively confining the stress to box, beneath the glass and above and slightly beyond the embedded vias pad surface.

This force is distributed over a small area creating high pressure, which is directly related to the thickness of the resin between the pad surface and the glass layer. If this pressure exceeds the strength of the resin material, delamination will result. This delamination is often catastrophic, in that it effects an area(s) large enough to be seen as visible blisters on the surface of the board.

Stress Zone 2: This region is similar to stress zone #1, but extends beyond the first glass layer. This recognizes that in standard HDI boards, the surface dielectric layers can deform also, which allows some of the stress to be distributed. When this region is capped with copper in HDI boards (as illustrated) or blind vias are laminated next to another fully cured subcomposite, the deformation is diminished significantly. This minimizes the ability of the structure to reduce stress, effectively increasing the Stress Zone #1.

This is the cause of "eyebrow" cracks in HDI boards, and part of the reason blind via boards (as defined above) are more likely to delaminate than other PCB structures.

Stress Zone 3: This region is similar to stress zone #2 on HDI boards, but now has a microvia on top of the buried via. The buried via pad deformation, along with the dielectric swelling stress, try to push/pull the microvia off of the landing pad. The defect is opens between the microvia on the surface and the buried via below.

Also, if the material fractures or delaminates, it will also often cause a open circuit at this location.

Ways to Improve Designs and Fabrication

High-level Overview:

1. Reduce structural stress
2. Distribute stress over larger area
3. Use fracture resistant or tougher materials

Material selection:

- **Subparts:** Low Z-axis expansion is preferred as it reduces CTE mismatch stress. High Tg is generally helpful, as it normally reduces stress. However, some very hard High-Tg materials may increase stress.
- **Surface dielectrics (or between blind subparts):** Low modulus materials, particularly when subpart material hits Tg. For example, Tg should be equal or lower on these layers.

Stack-up:

- **Subparts:** Go to lowest reliable resin content. This reduces Z-axis expansion.
- **Surface dielectrics:** Choose a resin content high enough to prevent glass stop, which spreads the stress over a larger volume/area. The amount of resin coating over the copper pad depends on material hardness/brittleness. The softer or fracture-toughened the material, the thinner the resin coating can be.

If multiple plies are used, but the highest resin filling capability, thinnest glass against the copper layer.

Design:

- **Circuit area on subpart surface bonding layers:** This is the most important design impact. Low retained copper circuit areas make up most of the delamination-prone designs in the industry. Retain as much copper on this layer and make it as uniform as possible. There are two reasons for this:
  1. More resin is required to fill the area between the circuits, leaving less for forming a good resin layer over the pad surface.[1]
  2. Low copper circuit density, usually results in thicker copper plating on the traces, if pattern plating is used. This exaggerates the effect of reason one.
- **Copper coverage on surface dielectrics:** As noted above, solid fills on outer layers of finished PCBs can increase the likelihood of internal cracks. Whenever possible, avoid using filled area over buried vias.

Fabrication:

- **Stack-up:** Choose prepregs with sufficient resin to prevent glass stopping against subparts. Request copper fill on designs with low percentage of copper.
- **Subpart Plating:** Minimize surface copper thickness on subpart plating to minimize resin fill issues. Avoid overplating, use plating program that maximizes throwing power and surface distribution, or use surface copper thinning.
- **Oxide:** These designs affect oxide processing in two ways:
  1. A higher adhesion is needed to prevent delamination.
  2. Many alternative oxides do form a lower capability bonding surface on plated copper.

General

These designs are much more prone to moisture-induced delamination. Use all best practices in reducing moisture levels in fabrication, packaging and assembly use

Footnotes

[1] Resin filling of the areas between circuitry is a critical consideration. Basically, you take the percentage of copper free area multiplied by the copper thickness, this is the amount of resin needed to fill between the circuitry.

Examples:

- 0.5 oz copper, 50% retained copper
  Resin need = 50% (copper free area) x 0.6 mils (copper thickness) = 0.3 mils resin
- 0.5 oz copper, plated IPC, 50% retained copper
  Resin need = 50% (copper free area) x 1.2 mils (copper thickness) = 0.6 mils resin
- 0.5 oz copper, plated IPC, 10% retained copper
  Resin need = 90% (copper free area) x 1.4 mils (copper thickness) = 1.2 mils resin

If the prepreg being used has 0.5 mils available resin, you can see the impact of the design and plating. Remember, you want 0.2 mils or more resin available after filling.

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