# Improved High Speed, Low Loss Materials for Lead-Free Assembly Compatibility

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**Abstract**
Environmental regulations such as the Reduction of Hazardous Substances (RoHS) act are forcing the elimination of lead (Pb) from electronic equipment. Lead-free solders currently being used and developed for printed circuit assembly require higher processing temperatures that can degrade the base materials commonly used in printed circuits, resulting in decreased long-term reliability. The higher temperatures also result in greater amounts of Z-axis thermal expansion in the printed circuit board. This increased thermal expansion results in greater stress on plated through holes in the printed circuit board which also negatively impacts long-term reliability. Following a brief discussion of the lead-free solder materials and processes, this paper will review several base material properties that are critical to specify when transitioning to lead -free assembly. These properties include the glass transition temperature, coefficients of thermal expansion, decomposition temperature, and times to delamination. This paper will then compare the properties of a new low Dk, low Df material with an existing low Dk, low Df material in widespread use.

**Introduction**
There has been a long debate regarding the benefits of the elimination of lead from electronic equipment. It is not our intent in this paper to enter into this debate, as it is clear that the transition to lead-free assembly materials is well underway. Rather, our intent is to provide data on materials developed to meet the reliability requirements of current electronic products that will be assembled at higher temperatures that, other things being equal, have a negative impact on product reliability.

Many alternatives to Sn/Pb, the standard solder used for most electronic products, have been developed. However, it appears that Sn/Ag/Cu (SAC) alloys will be the most widespread. The advantages of SAC include the availability of the raw materials, the relative simplicity of the alloys, and the relatively low cost. The major disadvantage to SAC is the higher melting point of these alloys compared to Sn/Pb. The melting point of SAC is about 217$^{o}$C, or approximately 34$^{o}$C higher than Sn/Pb, which has a melting point of 183$^{o}$C. For proper wetting and solder joint formation with Sn/Pb solder, it is common to see peak reflow temperatures of 230-235$^{o}$C, or about 43-48$^{o}$C above the melting point. Assuming a similar temperature above melting is required for SAC, this implies that peak temperatures for lead-free assembly could approach 260$^{o}$C. Coupled with ever-increasing printed circuit board complexity and the potential rework cycles associated with complex designs, the higher temperatures will clearly place additional requirements upon the base materials used to manufacture the printed circuit. Prior work[i] has discussed in some detail the critical base material properties with respect to lead-free assembly. Therefore, only a brief review is presented here.

**Critical Base Material Properties**
Three critical base material properties with respect to lead-free assembly are the glass transition temperature (Tg), thermal expansion, and decomposition temperature. The Tg is viewed by many as a proxy for overall material reliability. The prior work referenced above explains why this is an overly simplistic view which can actually lead to poor material choices for lead-free assembly applications. The primary reason that Tg is important is due to its effect on overall thermal expansion within a given temperature range. Because rates of thermal expansion below Tg are much lower than rates of expansion above Tg, other things being equal, a material with a higher Tg will exhibit less overall expansion within a given temperature range than a material with a lower Tg. However, as illustrated in Figure 1, it is possible for a lower Tg material to exhibit less total expansion than a higher Tg material because of lower rates of thermal expansion.

Therefore, the rates, or coefficients of thermal expansion (CTEs) are also a critical property to consider. The CTEs are calculated from the slopes of the linear portions of the curves above and below the inflection points. The slope below this point is the pre-Tg expansion rate (pre-Tg CTE) and the slope above this point is the post-Tg expansion rate (post-Tg CTE). As noted above, less total expansion results in less stress on plated through holes and therefore improved reliability.

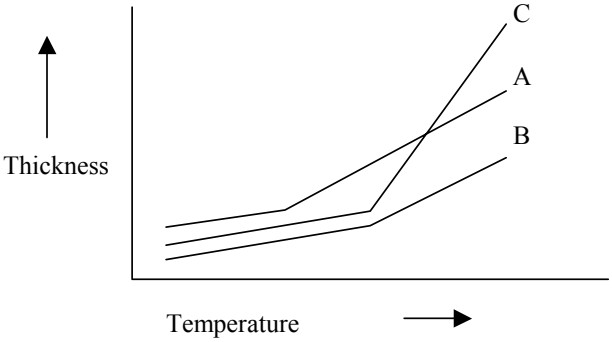


**Figure 1 – Impact of Tg and CTE Values on Total Expansion**

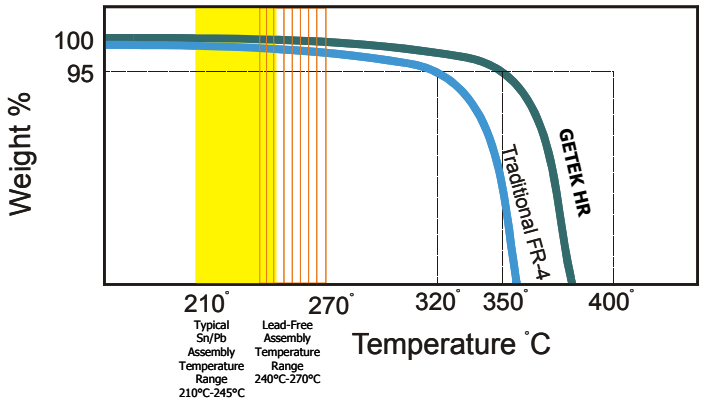


**Figure 2 – Decomposition Curves for Standard FR-4 and a New Low Dk/Df Material**

Base material decomposition temperature is a fundamental property that has not been discussed in great detail over the years. However, this property is very important to understand as products are converted to lead-free assembly. The decomposition temperature is defined as the temperature at which 5% of the original mass of a sample is decomposed. A thermogravimetric analysis (TGA) system is used to measure this property. A sample is placed in the TGA unit which measures the sample mass as the temperature is increased. Initially, any absorbed moisture or other volatile compounds may be driven out of the sample, reducing the sample mass. The amount of volatiles are typically no more than 0.5% of the sample mass, but can vary somewhat across material types. At higher temperatures, the chemical bonds within the resin system will begin to break and oxidation of the resin system components will result in the by products being volatilized from the sample, reducing its mass further. Figure 2 compares two different laminate materials, one a standard FR-4 material, the other a new low Dk/Df product. The traditional FR-4 has a measured decomposition temperature of 320°C while the new low Dk/Df material has a decomposition temperature of 350°C.

However 5% decomposition is fairly high, especially if a printed circuit is going to be exposed to multiple assembly and rework cycles. The shaded regions of Figure 2 illustrate why exposure to lead free assembly temperatures are cause for concern. The yellow region highlights the temperature range where traditional tin-lead solder assembly takes place. In this region, neither material exhibits significant decomposition. In the lead-free temperature range, however, traditional FR-4 materials can exhibit 1-3% decomposition. With multiple thermal cycles, this can severely degrade long-term reliability or even cause defects such as blisters, measles, or delamination in the assembly process. Materials with higher decomposition temperatures exhibit little-to-no decomposition in the lead-free assembly temperature range, and are therefore more robust in terms of both assembly reliability and long-term reliability. Prior work comparing FR-4 products has validated this correlation[i].

**Properties of the New Low Dk/Df Material**

One of the most common low Dk/Df materials used in high performance printed circuits uses an epoxy/PPO resin system (GETEK®). The new low Dk/Df material (GETEK® HR) also uses an epoxy/PPO resin system, but has been engineered to exhibit significantly reduced levels of thermal expansion. Figure 3 provides a comparison of these two products and also includes a thermal expansion curve for a 180°C Tg, lead-free compatible FR-4 for reference. Clearly, the 'standard' low Dk/Df material exhibits a relatively high level of thermal expansion in the range of 50-250°C. The lead-free compatible FR-4 and the new low Dk/Df material exhibit significantly lower levels of thermal expansion. Note that these products exhibit the same nominal Tg, but different levels of overall thermal expansion because of the different rates of expansion (CTEs), especially above the Tg.

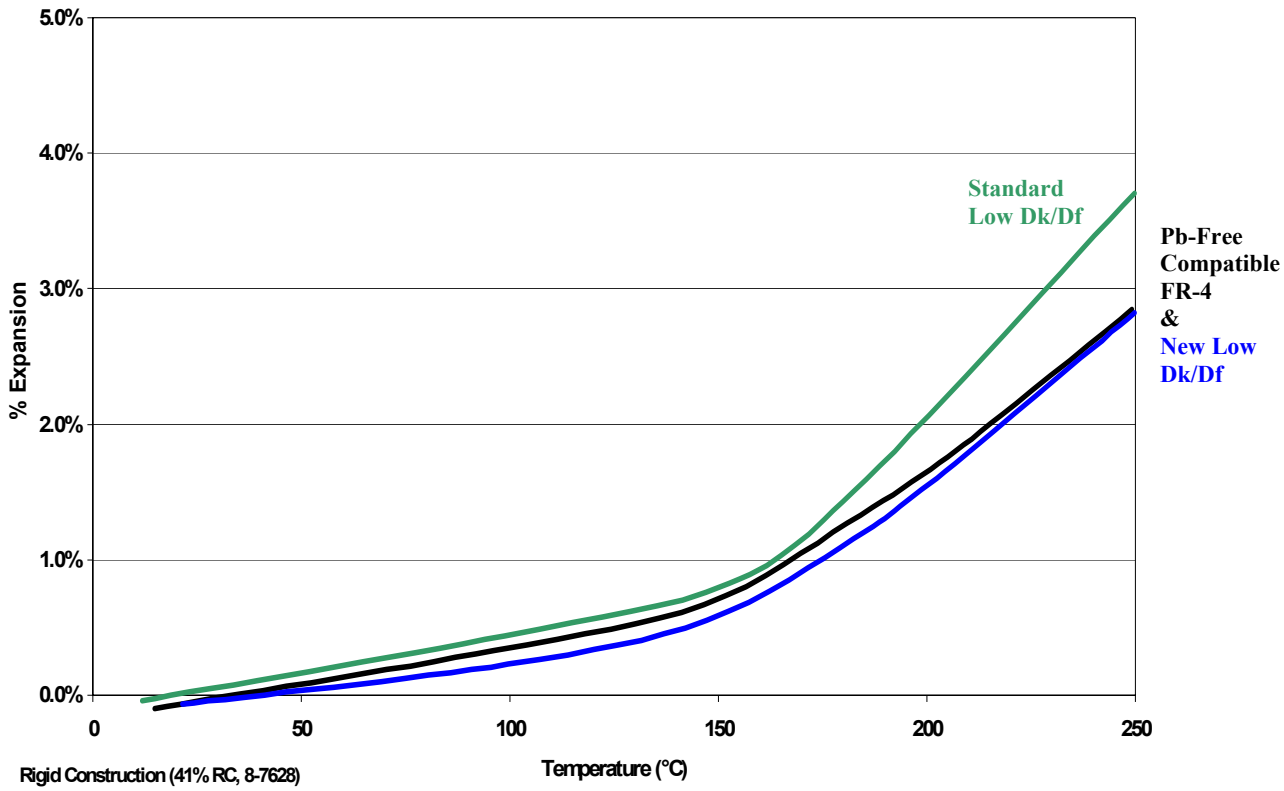


**Figure 3 – Comparison of Overall Thermal Expansion**

**Table 1 – Properties of Common Materials and the New Low Dk/Df Substrate Material**

| Property | Std. 140°C Tg | Std. 175°C Tg | Pb-Free 150°C Tg | Pb-Free 180°C Tg | Std. Low Dk/Df | New Low Dk/Df | Very Low Dk/Df |
|---|---|---|---|---|---|---|---|
| DMA Tg, °C | 140 | 175 | 150 | 180 | 180 | 180 | 200 |
| Pre-Tg CTE, ppm/°C | 50 | 50 | 45 | 45 | 60 | 41 | 55 |
| Post-Tg CTE, ppm/°C | 250 | 250 | 230 | 220 | 280 | 230 | 225 |
| % Expansion, 50-260°C | 4.2 | 3.5 | 3.4 | 2.7 | 3.7 | 2.8 | 3.2 |
| Decomposition Temp., °C | 320 | 310 | 350 | 350 | 350 | 350 | 400 |
| Dk @ 1 GHz | 4.3 | 4.4 | 4.5 | 4.5 | 3.9 | 4.0 | 3.5 |
| Dk @ 5 GHz | 4.2 | 4.3 | 4.4 | 4.4 | 3.8 | 3.9 | 3.45 |
| Df @ 1 GHz | 0.016 | 0.016 | 0.017 | 0.017 | 0.009 | 0.009 | 0.006 |
| Df @ 5 GHz | 0.017 | 0.018 | .0185 | 0.0185 | 0.010 | 0.010 | 0.007 |

Table 1 provides data on several common materials, as well as the new low Dk/Df material. For the Dk and Df measurements, samples with 50% resin content were measured. All other data is based on laminates with 40% resin content. The standard 140°C Tg material and the standard 175°C Tg material are currently used in lead-free applications, but with limitations. These limitations are due to the lower decomposition temperatures and the high thermal expansion of the 140°C Tg material. Suitability for lead-free applications will depend on the printed circuit design as well as the actual thermal profiles the circuits will be exposed to during assembly. All of the other products exhibit higher decomposition temperatures, and with the exception of the standard low Dk/Df product, relatively low levels of thermal expansion. The "Pb-Free 150°C Tg" material and the "Pb-Free 180°C Tg" material are currently being used in lead-free assembly applications in a broad

range of printed circuit designs and assembly profiles with very good results. As you can see from the table, the "Pb-Free 180oC Tg" material and the New Low Dk/Df material exhibit very similar thermal properties.

Next, a multilayer printed circuit design was chosen for comparison of the standard and new low Dk/Df products. The circuit contained 10-layers and had an overall thickness of 2.3 mm (0.090"). Table 2 summarizes the data collected from these multilayer printed circuits.

**Table 2 – Thermal Analysis of Standard and New Low Dk/Df Materials**

| Property | Std. Low Dk/Df, With Copper | Std. Low Dk/Df Without Copper | New Low Dk/Df With Copper | New Low Dk/Df Without Copper |
|---|---|---|---|---|
| Pre-Tg CTE, ppm/°C | 69 | 70 | 53 | 61 |
| Post-Tg CTE, ppm/°C | 335 | 365 | 310 | 340 |
| % Expansion, 50-260°C | 4.3 | 4.7 | 3.5 | 4.2 |
| T260, min. | 23.8 | 30+ | 30+ | 30+ |
| T288, min. | 1.1 | 10.9 | 3.5 | 15.3 |

The samples listed 'with copper' were taken from an area of the multilayer printed circuit board that contained copper on the various layers of the circuit. Samples listed 'without copper' were taken from an area of the circuit where there was no copper on any of the layers of the multilayer circuit. The areas without copper will contain a higher resin content than the areas with copper, which results in higher levels of thermal expansion. In addition, in multilayer printed circuits the resin content is generally much higher than the resin content in laminates, which explains why the expansion values in Table 2 are higher than the expansion values in Table 1.

From this data, it is clear that the new low Dk/Df material exhibits significantly less thermal expansion than the standard low Dk/Df material. Time to delamination data is also provided in Table 2. The time to delamination test brings a sample to a specified temperature, 260°C in the case of the T260 and 288°C in the case of T288, and measures how long it takes for delamination to occur. The delamination will typically occur between the resin and copper, resin and fiberglass reinforcement, or in the case of multilayer printed circuits, between the resin and the innerlayer copper surfaces. In the T260 data presented above for the multilayer PCB, only the standard low Dk/Df material in the area with copper fails to reach 30 minutes without delamination. All other samples reached 30 minutes, at which point the test was stopped. In comparison, most multilayer printed circuits manufactured with standard high-Tg FR-4 materials fail within 1.5 to 4 minutes (the high-Tg FR-4 materials developed for lead-free assembly will last significantly longer). In the T288 testing, the new low Dk/Df material lasts significantly longer than the comparable samples of the standard low Dk/Df material. Multilayers made from standard high-Tg FR-4 materials often do not even make it to the 288°C temperature before delaminating, or if they do, they do not last very long (again, the high-Tg FR-4 materials developed for lead-free assembly will perform better than the standard high-Tg FR-4 materials).

Further assessments of lead-free compatibility are also underway. These include thermal cycling tests that measure the change in properties of the materials versus the peak temperature experienced, and number of cycles of exposure to the peak temperature. Measures of both assembly reliability and long-term reliability are also underway. The assembly reliability tests will evaluate resistance to blistering, measles and delamination during assembly processes. Initial long-term reliability assessments will utilize interconnect stress testing (IST)[ii] that includes sample preconditioning to lead-free temperatures. This data will be presented once it is complete.

**Conclusions and Summary**

From the data presented above, it is obvious that the properties of the new low Dk/Df material are improved from the standard low Dk/Df material. In particular, significant reductions in thermal expansion characteristics have been realized while maintaining the excellent electrical properties. The high decomposition temperature, another important property for lead-free assembly compatibility, is also maintained. Finally, better performance in time to delamination tests are also realized. In summary, the improvements realized in the new low Dk/Df material increase the compatibility of the new material with lead-free assembly processes.

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[i] Kelley, Edward, An Assessment of the Impact of Lead-Free Assembly Processes on Base Material and PCB Reliability, APEX/IPC Conference, 2004.

[ii] Procedure developed and offered through PWB Interconnect Solutions, Ottawa, Ontario, Canada.