

Signal Integrity Considerations in High-Reliability Designs

Tarun Amla, Sean Mirshafiei

Acknowledgments

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References

1. Howard Johnson, High Speed Signal Propagation: Advanced Black Magic, Prentice Hall 2003
2. Eric Bogatin, Signal Integrity-Simplified, New Jersey Prentice Hall Modern Semiconductor design series 2004
3. Tom Granberg, Handbook of Digital Techniques for High-Speed Design, New Jersey, Prentice Hall Modern Semiconductor Design Series 2004
4. Josef Bicerano, Prediction of Polymer Properties, Marcel Dekker, 2002

Authors:

Sean Mirshafiei is the Director of High Speed Digital products for Isola Group. He can be reached at Sean.Mirshafiei@isola-group.com
Tarun Amla is Vice President and Chief technology Officer for Isola Group. He can be reached at Tarun.Amla@isola-group.com

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Abstract

With the advent of ROHS legislation, there has been an ever increasing focus on lead-free compatible materials. Lead-free alloys have higher liquidus temperatures; therefore, assembly temperatures have shifted upwards anywhere from 20°C to 40°C. This imposes new challenges on base materials, which are now expected to withstand high assembly temperatures. The common solutions so far have focused on phenolic-cured systems which enhance the thermal properties over the conventional epoxy systems cured with Dicy. Phenolic-cured systems, while capable on the thermal front, have limited use for higher speed applications due to high dielectric properties and higher loss. High Tg dicy-cured materials, while capable of delivering performance on the electrical front, are not very capable of delivering performance on the thermal front. Higher performance materials using non-epoxy chemistries may be suitable as far as thermal and mechanical attributes are concerned, but these may not be a fit for many cost-sensitive, mainstream applications.

This article outlines the challenges for lead-free designs with demanding signal integrity requirements while managing cost constraints. The article also attempts to dispel the perception that signal integrity material challenges only exist with very high-speed applications, requiring long transmission lines.

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Signal Integrity Considerations in High Reliability Designs

Over the past several years OEMs, contract manufacturers, PCB fabricators, and material suppliers have been tackling the issues that arose once the European Union passed the RoHS and WEEE legislation. One aspect of the legislation was the restriction of lead from electronics, which subsequently led to changes in assembly processing of PCBs. For a majority of lead-free assembly applications, traditional dicy-cured FR-4 materials have been shown to perform poorly during lead-free assembly or have significantly deteriorated thermal reliability after lead-free assembly. The laminate industry has responded with numerous types of lead-free compatible FR-4 materials based on a phenolic-cured chemistry. These materials have generally been robust during lead-free assembly and demonstrated improved long-term reliability. Although the needs of thermal performance appear to have been met, the impact these new materials have on signal integrity needs further consideration.

Dicy-cured products start decomposing at fairly low temperatures and as such are not deemed suitable for high-temperature assembly applications. The phenolic-cured products are not very suitable for higher speed applications, as dielectric properties are different when compared to the standard dicy-cured products.

Technology Drivers Signal Integrity

Several years ago the highest frequency encountered in digital circuits was below 20 MHz; since then the definition of high-speed digital transmission has changed immensely. Simply put, the basic idea in digital transmission is to communicate information between a driver and a receiver with signals representing binary bits of information. These bits are encoded on a leading and or trailing edge of a wave form; typically high voltage is one and low voltage is zero. The conductive paths between the chip

that sends the signal to the receiving chip are called interconnects. A group of interconnects represents a bus. The rise time (RT) or edge rate is defined as the time a signal takes to achieve certain amplitude. For example, RT10-90 is defined as the time required for the signal to change from 10% to 90% of its peak value. Digital designs have continued to experience significant increases in clock frequency and reductions in edge rates. The result of these advancements is that circuits as short as a few inches begin to act as transmission lines. These transmission lines act to both delay and attenuate signals as they travel between the source and termination. In addition to considering the clock frequency and edge rates of microprocessors, high-speed telecommunications equipment utilizes ever-increasing data rates that correspond to higher clock frequencies. For example, the OC-48 (Optical Carrier) operates with a data rate of 2.5 Gbps. The relationship between data rate and clock frequency depends on the method of bit encoding on the signal. In some cases the relationship of bit rate and clock frequency is 1:1. In the example of an OC-48, a 1:1 relationship would translate to a clock frequency of 2.5 GHz. At high frequencies, dielectric materials influence signal propagation and degree of attenuation. Material properties available to signal integrity engineers from laminators are generally limited to the permittivity (ϵ_r) and dissipation factor ($\tan\delta$). Permittivity or dielectric constant is a dimensionless number that compares the permittivity of the medium to free space. Dissipation factor or loss tangent defines the energy dissipated into the medium due to polarization.

Despite having this data available, many PCB fabricators and laminators struggle to apply this information when asked to recommend a material to designers for a specific application. One approach shown to be successful requires laminators and fabricators to collect “real world” performance data on various materials using equipment and measurement techniques

employed by designers. In addition, the parties need to consider the factors that influence signal quality and how signal quality is measured. As a result there are quite a few perceptions in the user community such as:

- Marginal differences in electrical properties of phenolic and dicy-cured systems; therefore, dicy-cured and phenolic systems are interchangeable for most applications.
- Differences in dissipation factor are only relevant for very high-speed applications
- Differences in dissipation factor are only relevant for very long transmission lines.

We will explore each one of these perceptions.

Interchangeability on Stack-Ups

Table 1 presents properties of dicy-cured FR-4 materials and their lead-free compatible counterparts.

Table 1. Hi-Tg FR-4 Material Properties

| Material Properties | Dicy-Cured FR-4 | Un-Filled Phenolic Lead-Free Comp. FR-4 | Filled Phenolic Lead Free Comp. FR-4 | Non-Phenolic Lead-Free Comp. FR-4 |
|----------------------------|-----------------|---|--------------------------------------|-----------------------------------|
| Tg | 170C | 180C | 180C | 200C |
| Td (5% wt Loss) | 300C | 350C | 340C | 370C |
| CTE _z (40-260C) | 4.40% | 3.50% | 2.80% | 2.80% |
| Dk (2 GHz) | 3.79 | 3.76 | 4.04 | 3.7 |
| Dk (5 GHz) | 3.76 | 3.69 | 3.92 | 3.68 |
| Dk (10 GHz) | 3.76 | 3.69 | 3.92 | 3.68 |
| Df (2 GHz) | 0.0180 | 0.0210 | 0.0210 | 0.0135 |
| Df (5 GHz) | 0.0186 | 0.0250 | 0.0250 | 0.0138 |
| Df (10 GHz) | 0.0186 | 0.0250 | 0.0250 | 0.0138 |

As illustrated, permittivity does vary significantly between dicy-cured and filled phenolic-cured systems; the typical difference between dicy-cured and filled phenolic-cured systems is approximately 8%. Filled phenolic-cured systems have higher Dk values, as almost all suitable inorganic fillers possess dielectric constants above 3.8. Since the dielectric constant of materials follows a volumetric

relationship, permittivity moves up by 8-10%. This change is not insignificant and may require a stack-up change or adjustment of the line width on existing designs to achieve the same desired impedance.

The option to change line width is not desirable since it entails a reduction in line width. Conductor losses are a function of the type of conductor, surface roughness, and most importantly, line width. If line width decreases we see a higher level of attenuation due to an increased skin effect. The skin effect is caused by the self-inductance of the conductor, resulting in an increase in the inductive reactance at high frequencies, which forces the current to flow on the skin of the conductor. The option to change stack height potentially introduces increased cost, reduced reliability, and fixturing issues.

Loss tangent values are also significantly higher for the phenolic-cured systems. Phenolic-cured systems have a much higher percentage of polar functionality. Polymer modeling with QSPR (Quantitative structure-property relationships) tools have shown that “-OH” functionality contributes heavily to the polarity of the systems and adversely affects dielectric properties. While it is not uncommon to see relatively low dissipation factor values published by several suppliers, these low values are the result of either inappropriate test methods and/or extrapolations. Our testing of multiple systems using the Bereskin Stripline Test Method for characterization and using modeling tools has shown that the phenolic-cured systems are inherently “lossy.” These numbers have been used in models and have shown very good agreement with the actual measurements; other methods normally tend to understate the loss of a system.

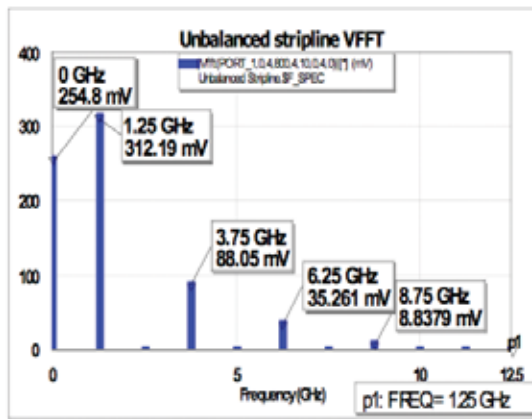
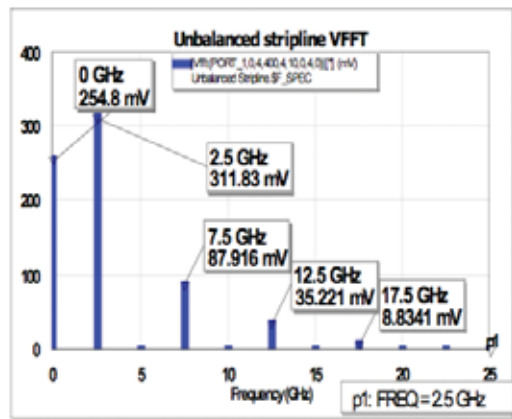
Time Domain Analysis

Signal integrity analysis occurs in both time and frequency domain. Examples of time-domain analyses include the measurements of edge rates,

jitter in an eye pattern, evaluation of the margin in an eye pattern around a jitter mask, and BERT (bit error rate testing).

One of the reasons for analyzing the edge rates of signals is to determine the frequency content of a signal. Signals are often described as overlapping sine-waves with differing frequencies. As shown in Figure 1, faster data rate signals are composed of higher frequency content signals, or sine waves. By overlapping these sine waves with increasing frequency, the desired edge rate is obtained.

Figure 1 Frequency Domain Analysis



By converting a signal from the time domain to the frequency domain using Fourier Transforms, signal integrity problems can be solved more rapidly. Signals in the time domain are characterized in

the frequency domain as sine waves with varying amplitudes, phases, and frequencies. The frequency spectrum is the range of frequencies necessary to describe the signal in the time domain. The bandwidth is the highest significant frequency in the spectrum used to describe the signal in the time domain.

The relationship between bandwidth (frequency domain) and rise time of a signal (time domain) is often characterized by the following approximation:

$$\text{Bandwidth(GHz)} = \frac{0.35}{Tr(n\text{sec})}$$

In general, this relationship means that as rise time decreases, bandwidth, or highest significant frequency, increases.

In order to obtain the frequency spectrum for a signal, a network analyzer is used to generate sine waves of varying frequencies and then transmit these waves through the device under test. The instrument is then used to determine how much of the transmitted signal reaches the destination. The transmission line is then characterized by plotting insertion loss as a function of frequency, as shown in Figure 2. The units for insertion loss are dB/unit length, or simply dB. The 3 dB bandwidth is the frequency that 70% of the amplitude of the signal still reaches the destination. This is illustrated as follows:

$$dB = 10 \log \frac{P_{out}}{P_{in}}, \text{ where } P \text{ is power (watts)}$$

also,

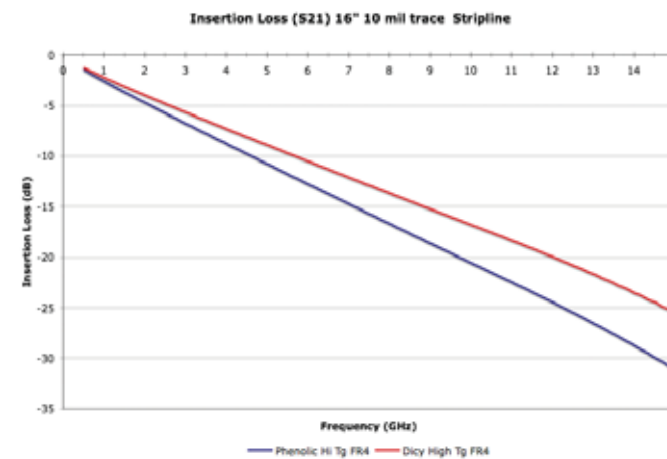
$$P = VI = \frac{V^2}{R} \text{ (Ohms Law)}$$

$$dB = 10 \log \left[\frac{\frac{V_{out}^2}{R}}{\frac{V_{in}^2}{R}} \right] = 10 \log \left[\left(\frac{V_{out}}{V_{in}} \right)^2 \right],$$

$$dB = 20 \log \frac{V_{out}}{V_{in}}$$

Figure 2 is a graphical representation of data generated on a 10-mil-wide, 16 in, 50Ω stripline. The chart in the figure illustrates that insertion loss of the same signal processed on a phenolic-cured high TG FR-4 is greater than that of a dicy-cured high TG FR-4. This is explained by the higher dissipation factor found with phenolic-cured materials. Depending on the design and required bandwidth, phenolic-cured high TG FR-4 may not be suitable for use based on the signal integrity requirements of the system.

Figure 2 Insertion Loss (S21) 10-mil-wide, 16 in stripline



Frequency Domain and Time Domain Analysis Using Phenolic-Cured Systems, Dicy-Cured Systems and Non-Phenolic Lead-Free FR4
Dielectric information was collected using Isola's Bereskin test method for Phenolic systems, Dicy cured High Tg systems and non-phenolic lead-free FR4. A simple linear function was used to fit the Dk/Df data with respect to frequency.

Interconnect Bandwidth Simulation Using Frequency Domain Analysis

Unbalanced striplines were modeled for the following configurations of 4 mil lines up to 4 in long. This would be typical of smaller line lengths for high-speed digital applications. Figure 3 shows a simple schematic of the simulation set up. A frequency sweep up to 15 GHz was used.

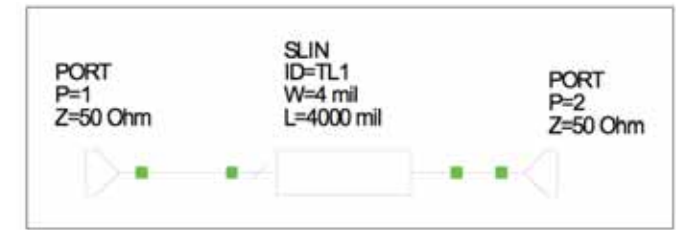


Figure 3 S21 parameters for the three types of materials tested.

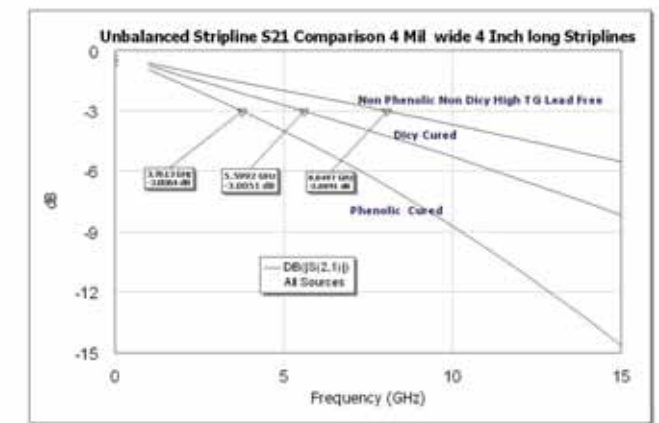


Figure 4 FR-4 Material 3 dB Bandwidth Comparison

We first looked at the 3-dB bandwidth. The bandwidth of an interconnect is the highest frequency it can handle without major degradation. Typically designers use a 3 dB bandwidth, which means the frequency component has lost 70% of its amplitude. Using the approximation of $RT = 0.35/\text{bandwidth}$ we get the estimate for rise time degradation.

One can see from the curve in Figure 4, that the phenolic-cured curve starts to droop steeply at higher frequencies, symptomatic of a higher dissipation factor at those frequencies.

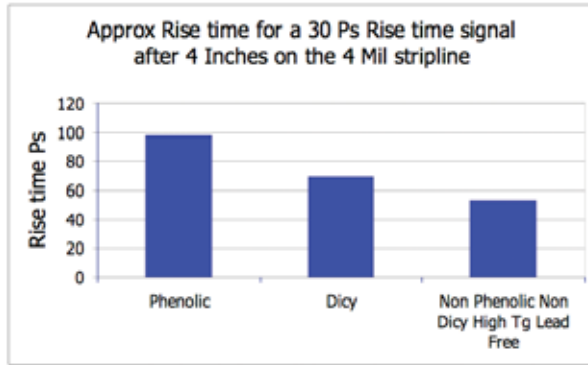


Figure 5 Approximate rise time for 30 Ps rise time signal after 4 in on 4 mil stripline.

The analysis in Figure 5 shows that for even seemingly benign distances, rise time degradation is severe when using phenolic-cured products, as compared to the current dicy-cured products and non-phenolic lead free FR4 products.

Time Domain Analysis

Eye diagrams are time domain representations of successive binary bits superimposed on each other. The schematic shown in Figure 6 was used to simulate an eye diagram. The characteristics of this transmission line are given as a 4-mil-wide stripline, 15 in long, operating at a 3.125 Gbps.

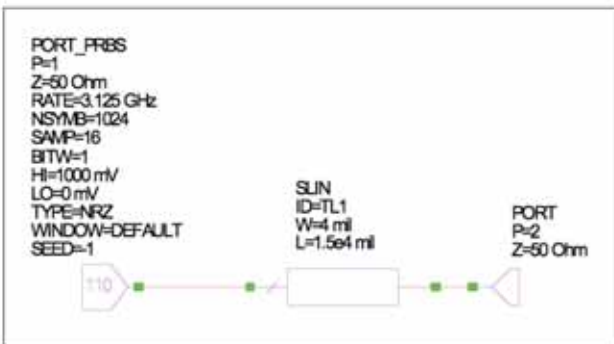


Figure 6 Schematic of a Single-ended Stripline structure

The eye diagrams were analyzed and characteristics such as jitter and eye opening

were extracted.

Figures 7, 8, and 9 show the results of the analysis

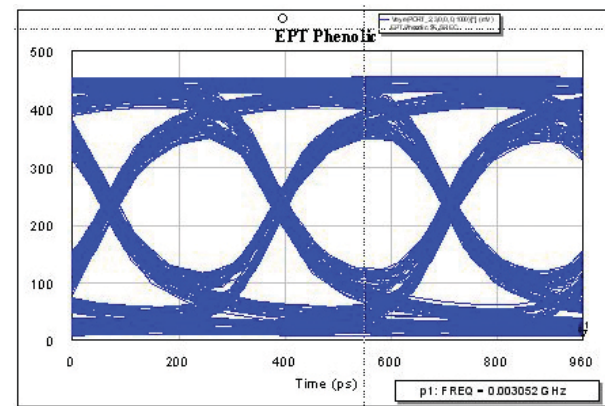
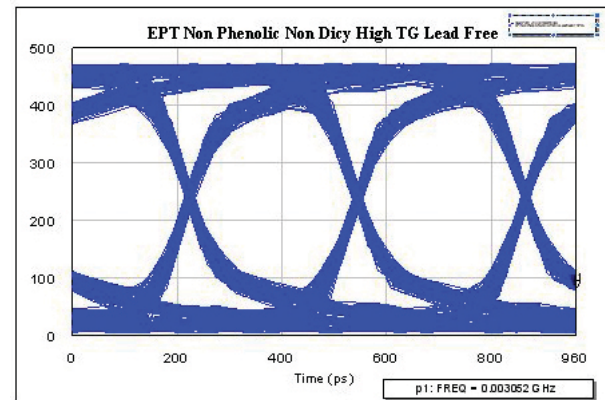
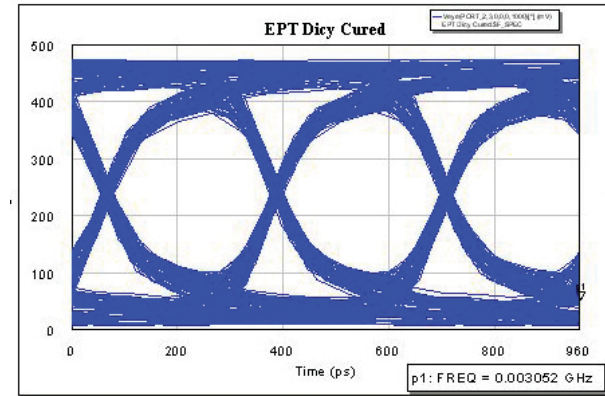


Figure 7 Eye Diagrams for phenolic-cured, dicy-cured, and non-phenolic lead-free FR4

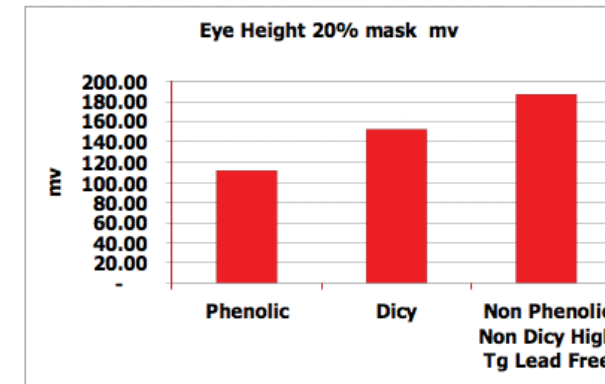


Figure 8 Eye height.

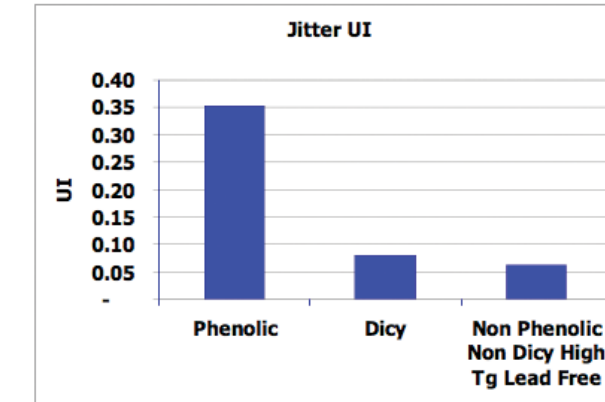


Figure 9 Jitter

Designers want to see reduced jitter (below a certain level of unit interval), low inter-symbol interference, and low bit error rate. The time domain analysis shown in Figures 7, 8 and 9 illustrate the degradation in performance when using phenolic-cured systems in place of dicy-cured systems. This degradation in performance severely limits the substitution of phenolic-cured materials for dicy-cured materials in high-speed digital designs currently in use.

Verification of the Models/Simulations

Microstrips were fabricated using various materials, and S parameters were generated using an Agilent PNA. Connector loss was accounted for by using two different sets of microstrips. The Dk and DF

numbers were extracted and found to be in very close agreement with the modeled numbers. Figure 10 shows the actual S parameter data. Wider lines were used to minimize the conductor loss and amplify the difference in dielectric loss numbers between materials



Figure 10 Attenuation (microstrip) comparison material types

Conclusions

Based on the analyses conducted, we feel that a simple substitution is not the answer for lead-free assembly conversion and there are significant signal integrity issues with phenolic-cured products such as:

- Higher dielectric constant leading to potential redesign issues such as stack height and line width changes.
- Higher attenuation leading to reduced bandwidth and degradation in rise times, regardless of line lengths
- High Tg FR-4 has been stretched to the limits by designers in high data rate applications. A substitution with phenolic systems would be a major step backwards.

There is a strong need in the market for cost-effective mid-Dk/Df systems that meet high-reliability requirements without compromising